

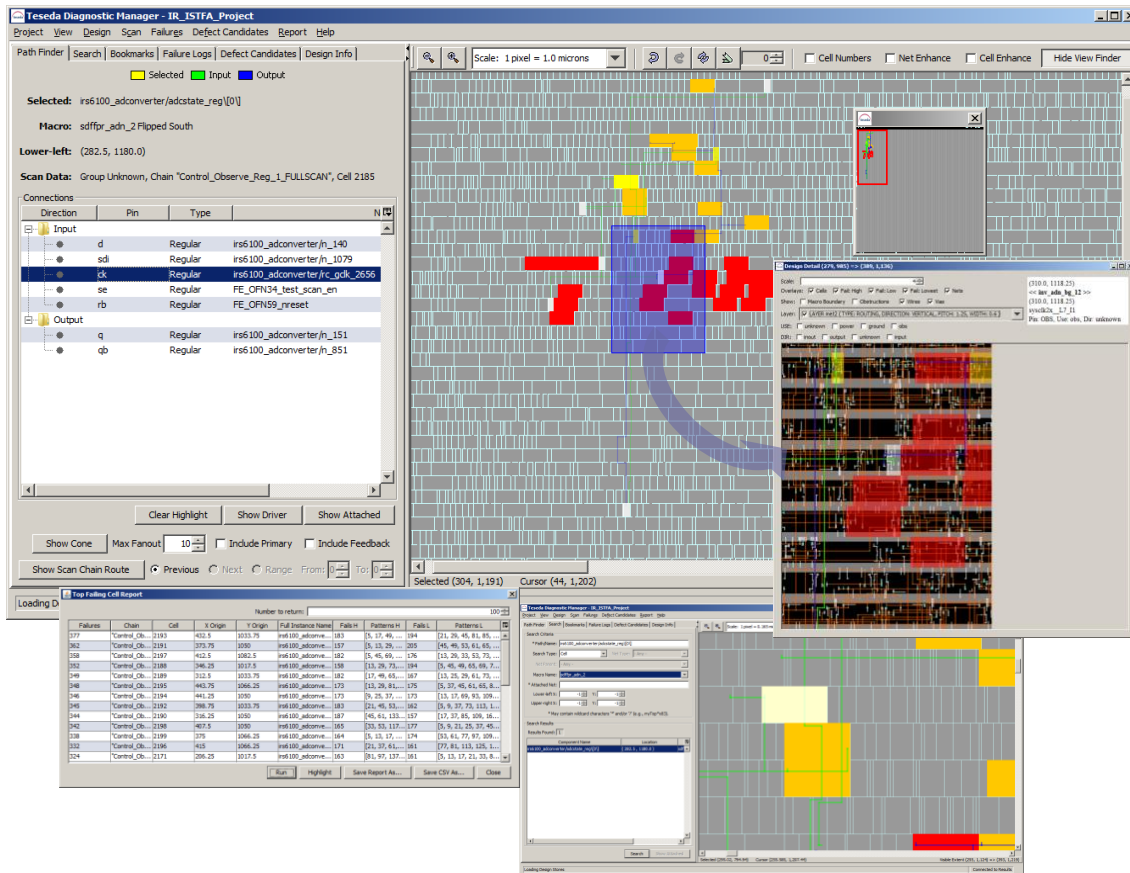


# Defect Isolator™

Isolate Defects to Root Cause in the Physical Environment

## Defect Isolator™ Highlights:

- Traverse through the physical design to trace nets and vias down to the defect location
- Utilizes industry standard LEF/DEF design files, scan-based test information, tester fail logs and diagnostic reports to determine and isolate the physical defect location
- Enables the user to leverage their diagnostic experience to determine the root cause of the defect
- Interactive layout viewer displays scan chains, mapped mismatches of scan cells, layers, nets and subnets with search capabilities (component, net, cell)
- Physical XY coordinates are always displayed for components and nets to guide the user through the design to quickly identify suspect sites for FA using techniques like Emission, OBIRCH, LIVA, TIVA, or FIB



## Key Benefits:

- Cuts defect localization time by up to 90%
- Maximize confidence of defect isolation *before* final destructive confirmation
- Rationalize to the defect root cause in one single tool environment
- Increase effectiveness, save time on expensive failure analysis imaging tools
- Reduces reliance on designer and EDA diagnosis tools

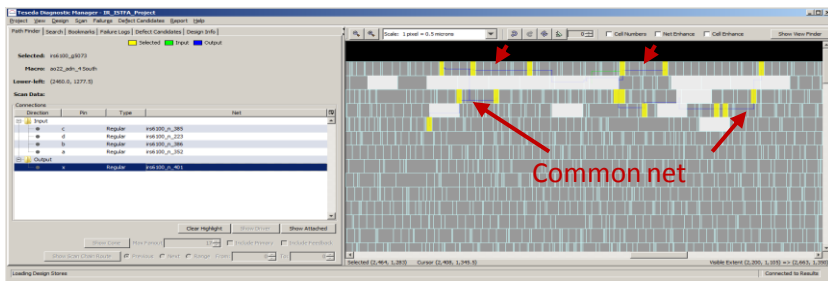
## Leveraging Scan and the User's Experience to Locate Defects Quickly

**Teseda Defect Isolator™** enables Product, Failure Analysis and Design Engineers to rapidly pinpoint the physical location of defects in silicon, reducing the dependence on expensive and time-consuming EDA diagnostic flows and external imaging tools. **Teseda Defect Isolator™** interprets physical design information, scan failure files, and highlights reported mismatches of failed test results captured in scan cells with the physical XY location in the device.

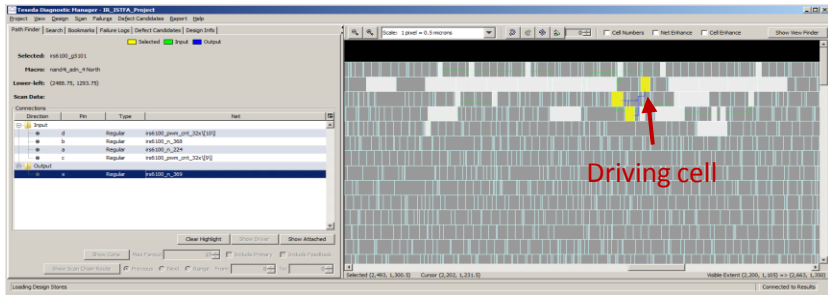
## Compatible with Industry Standard Formats

**Teseda Defect Isolator™** imports industry-standard LEF and DEF design files, Standard Test Interface Language (STIL) files and reads standard scan fail logs from the **Teseda Diagnostic Test Hardware™** or production ATE testers. **Teseda Defect Isolator™** supports diagnostic defect candidate lists from EDA diagnostic analysis tools.

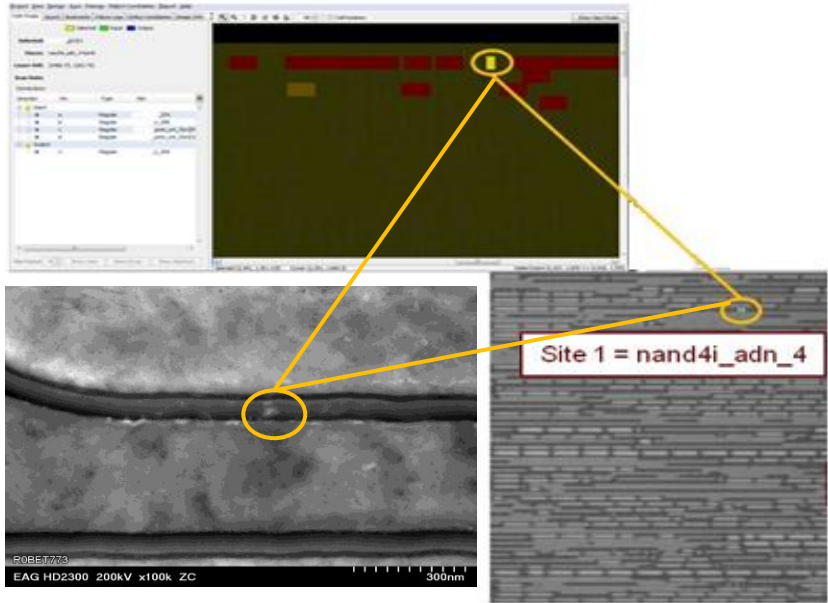
## Diagnose to the net, subnet, component pin with final confirm through FA techniques



Trace cones down to common nets or components

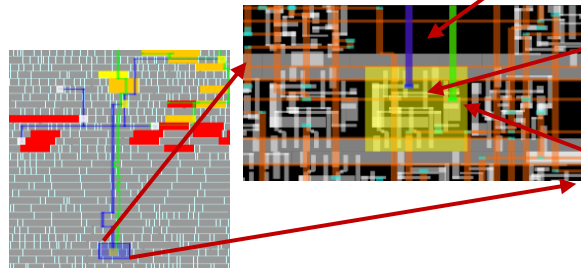


Identify driving cell of suspect net(s) and via(s)



Confirm with nondestructive (emission) or destructive (cross section or delayering) FA techniques for final confirmation

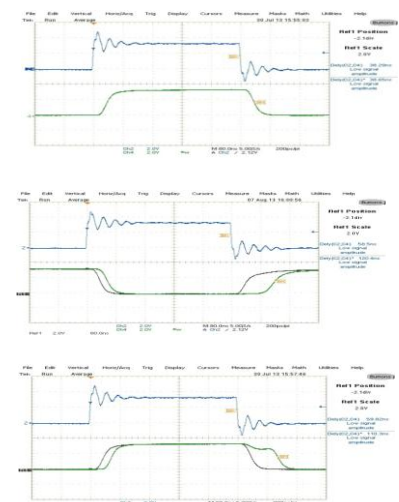
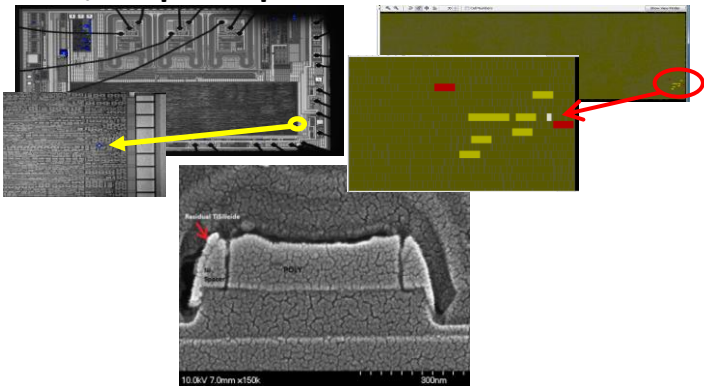
## Determine latencies in clock tree paths



## Defect Isolator™

- Patented algorithms for automated cone tracing and convergence provides a unique methodology for defect isolation
- Determine defect types: opens, resistive shorts due to residual silicide as well as latency timing issues
- Maps fail results to physical location of scan cells, nets, vias, and component internal structures
- Detailed viewer enables zooming of all physical elements of the design
- Search engine finds cells or nets of interest by cell or net name, macro type, region within the design, or attached net
- Highlight mismatching cells on the design to immediately visualize the defect area
- Bookmark cells of interest from the search engine or top failing cells report for future debugging

## Correlate exact XY coordinates of emission sites, FIB probe points and cross sections



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