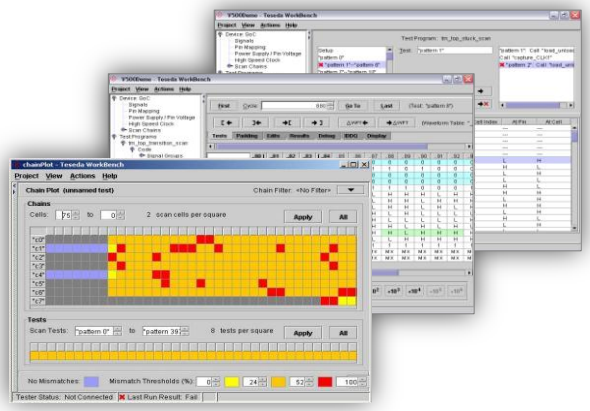
Teseda WorkBench™

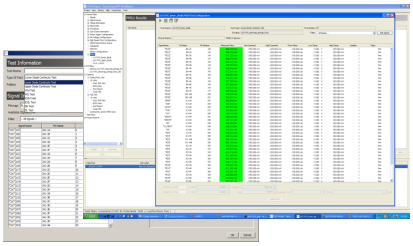
For Silicon Bring Up, Test Debug and Failure Analysis

Teseda WorkBench™ Highlights:

- Test control for the Teseda Diagnostic Test Hardware to perform scan-based testing, capture test results in pass/fail, failure capture and full capture modes of operation and display the test results graphically
- Graphic-oriented diagnostic features process display actual device test results, design hierarchy and scan-chain structure
- Run single or multiple tests consecutively with pause and looping control features
- Pattern data, clock and strobe edge placement editing
- Diagnose mismatching scan data to analyze and determine failing trends of behavior

Scan-Based Test and Debug
Stuck-At, Delay, IDDQ





DC Parametric Test
Characterize Force/Measure Current/Voltage

Controls
Diagnostic Test Hardware

Teseda WorkBench™

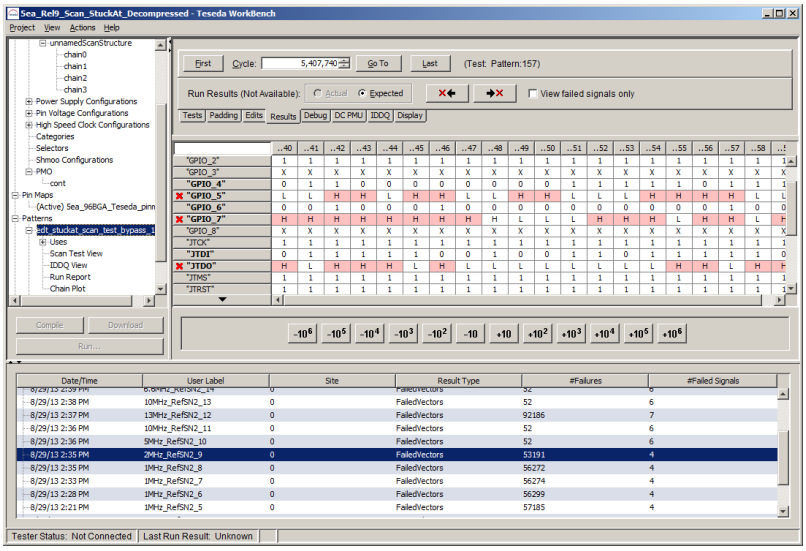
Key Benefits:

- Leverages scan to accelerate real-time interactive silicon validation, debug and failure analysis
- Boosts productivity and supports test and diagnostic flows with intuitive graphical user interface and design-based failure information
- Integrated scan validation graphically identifies problems with scan chains and scan tests for faster diagnosis
- Logical view displays scan cell placement of the design hierarchy

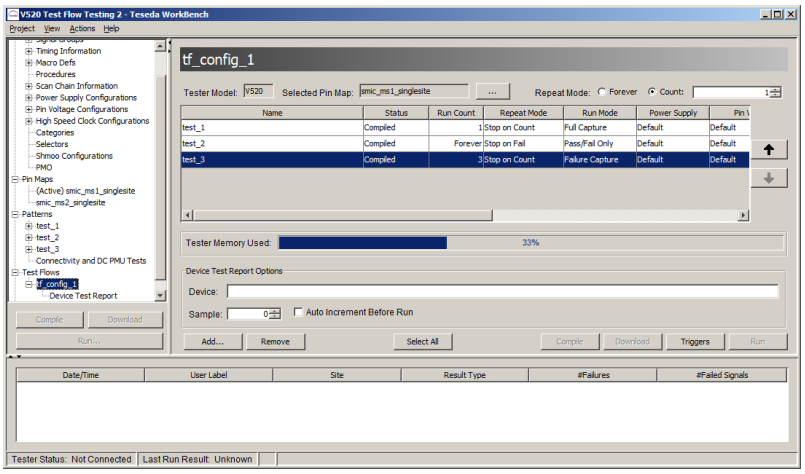
Interactive Scan-Based Testing and Device Stimulus for Failure Analysis

The **Teseda WorkBench™** software operates interactively on the **Teseda Diagnostic Hardware** desktop to provide fast, explicit, diagnostic information on scan failures in the hierarchical design. Design, test, manufacturing and FA teams can work together to reduce time in silicon bring up, device debug, production test and failure analysis diagnostics to isolate pattern and design issues, debugging of scan chains, accelerate yield learning and provide stimulus for defect isolation techniques in the FA lab. The **Teseda WorkBench™** preserves and understands the scan structures designed with EDA tools to identify specific problems in a meaningful context for the fastest results to further diagnose the logical test failures for further diagnosis downstream at the physical level in the FA lab. The net result is faster, more accurate failure diagnosis.

Scan-based test and debug to analyze behaviors of failing devices



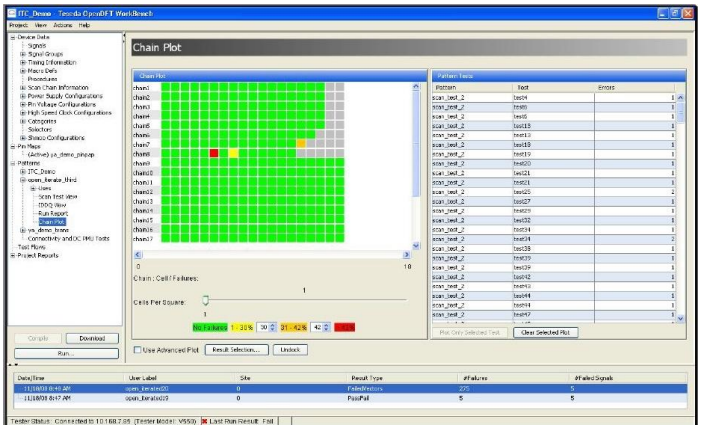
Diagnose mismatching scan cell for defect behavior



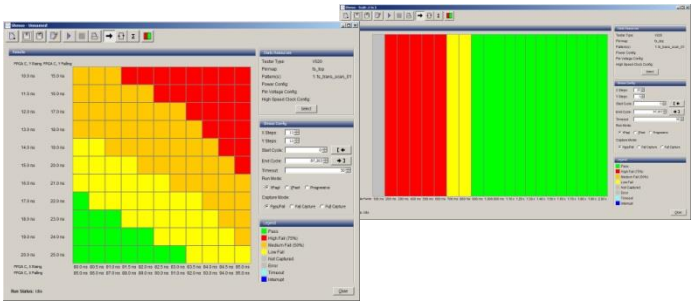
Run consecutive tests with repeat and looping capabilities

Teseda WorkBench™

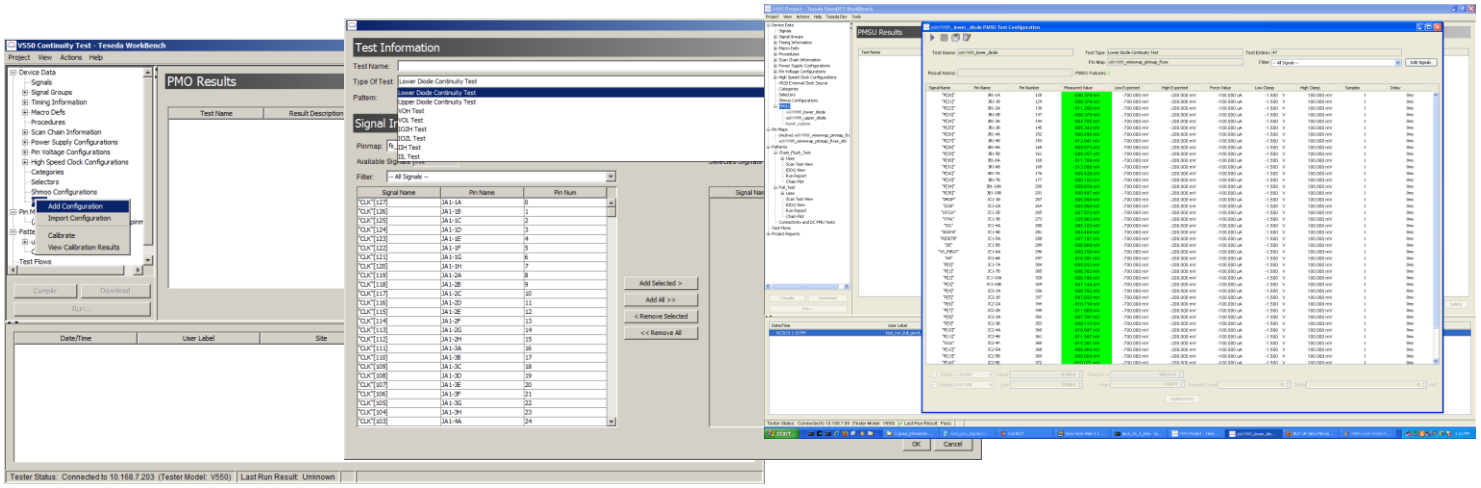
- Simple navigation through the test cycles quickly identifies scan mismatches by signal
- Supports IEEE 1450 Standard Test Interface Language files generated by ATPG tools from EDA vendors
- Generates scan failure logs in EDA formats
- Generates cycle logs highlighting failing cycles
- Displays for DC parametric test, IDDQ, Shmoo plot
- Pattern editing of pattern data, clocks and strobe



Chain Plot



Shmoo Plot



Continuity and DC Parametric Testing

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